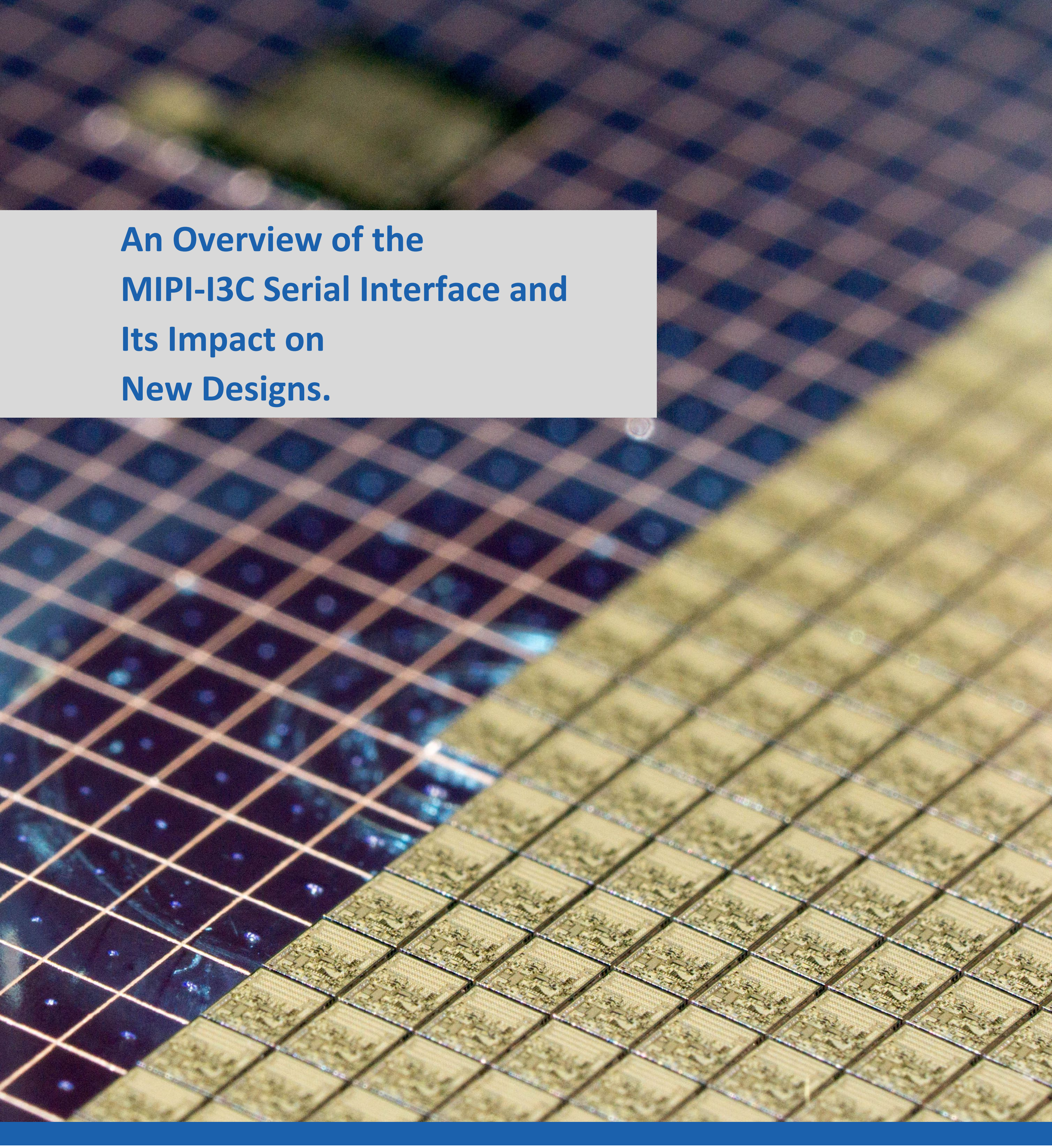

An Overview of the MIPI-I3C Serial Interface and Its Impact on New Designs.

SCT

SIGNAL CRAFT TECHNOLOGIES

Introduction

In recent years, the electronics industry has experienced an explosion in the growth of embedded sensors being used in high-volume applications such as smartphones, wearables, automobiles, and the Internet of Things (IoT). This rapid growth is fueled by the development of a wide variety of small-sized, low-cost sensors being married to an ever-expanding array of innovative consumer applications. An excellent example is today's typical smartphone, which incorporates 10 or more sensors measuring anything from light and biometric responses to motion and environmental conditions.

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To address these market needs, the MIPI I3C Standard was developed specifically to address connectivity between sensors and a host processor in mobile, wearable, and IoT applications. The I3C standard was collaboratively developed by MIPI's Sensors Working Group, which includes representatives from industry-leading companies such as AMD, Broadcom, Intel, NXP, and Qualcomm.

In November 2014, the Sensor Working Group first announced its goals for the I3C interface. Version 1.0 of the specification was released in December of 2017. Less than a year later, a significant number of companies are launching products incorporating the new interface standard.

While developing the standard, emphasis was placed on minimizing power consumption and increasing throughput, all while reducing PCB space and product cost.

MIPI I3C Scope and Purpose

The primary focus of I3C is to provide sensor connectivity in a highly efficient manner. While developing the standard, emphasis was placed on minimizing power consumption and increasing throughput, all while reducing PCB space and product cost. Other requirements included legacy I2C support and hardware simplification.

Legacy I2C Support

I3C is intended to be a superset of the I2C standard, capable of supporting the following five classes of devices. I3C devices will offer significantly enhanced functionality over legacy I2C devices.

- **I3C Primary Master** controls the I3C bus, which includes bus ownership control and hand-off to Secondary Masters.
- **I3C Secondary Master** can assume temporary control of the I3C bus, but requires permission from the Primary Master to do so. The Secondary Master will pass bus control back to the Primary Master upon completion of its task.
- **I3C Slave** responds to both common and individual commands from either I3C Primary or Secondary Masters.
- **I3C Peer-to-peer Slave** is a special class of device functionality in which a Slave can write to/read from another Slave without a Master's involvement. This is an I3C feature which could lead to significant power savings in certain applications.
- **I2C Slave** is a legacy I2C device existing on an I3C bus that can be controlled by an I3C Master. However, their speed and capabilities are constrained.

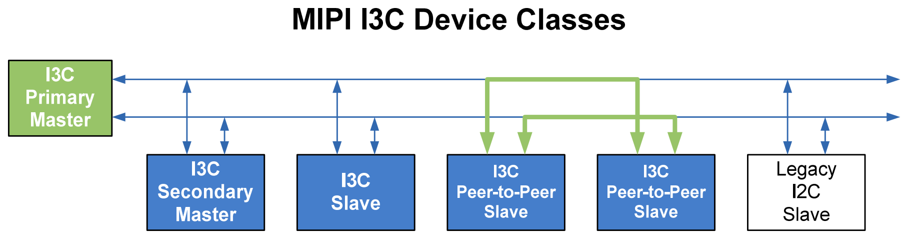

Figure 1. Functionalities of the REC and RE for the Downlink path (source: MIPI)

Enhanced Data Throughput

Data throughput similar to SPI speeds can be achieved with an I3C bus. A pure I3C bus is capable of data rates up to 26.7Mb/s, while a mixed I2C/I3C bus is limited to a respectable maximum rate of 20.5Mb/s. In contrast, a legacy I2C bus can support up to four different speed grades, with the fastest only achieving 3.4Mb/s, and the slowest of I2C slaves as little as 100kb/s. The I3C standard provides an additional four speed grades.

Mode	Description	Data Rate
Sm	I2C Standard mode	100kb/s
Fs	I2C Full-speed	400kb/s
Fm	I2C Fast mode	1 Mb/s
Hs	I2C High-speed mode	3.4Mb/s
SDR	I3C Standard Data Rate	10Mb/s
HDR-DDR	I3C High Data Rate - Double Data Rate	20Mb/s
HDR-TSL	I3C High Dara Rate - Ternary Symbol for Legacy Bus	20.5Mb/s
HDR-TSP	I3C High Data Rate - Ternary Symbol for Pure Bus	26.7Mb/s

Table 1. Summary of I3C and Legacy I2C Data Modes

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Simplified Hardware

Significantly reduced hardware complexity results from the simple two net I3C interface being shared by all I3C devices on the bus. A single bi-directional net consolidates transmit and receive data, and a second net supports the bus clock. The in-band interrupt capability of I3C eliminates the need for IRQ pins, typically required for each device. With sleep messages being part of the Common Command Code (CCC) set, device power management can enable and disable low power or deep sleep modes without the need of dedicated pins.

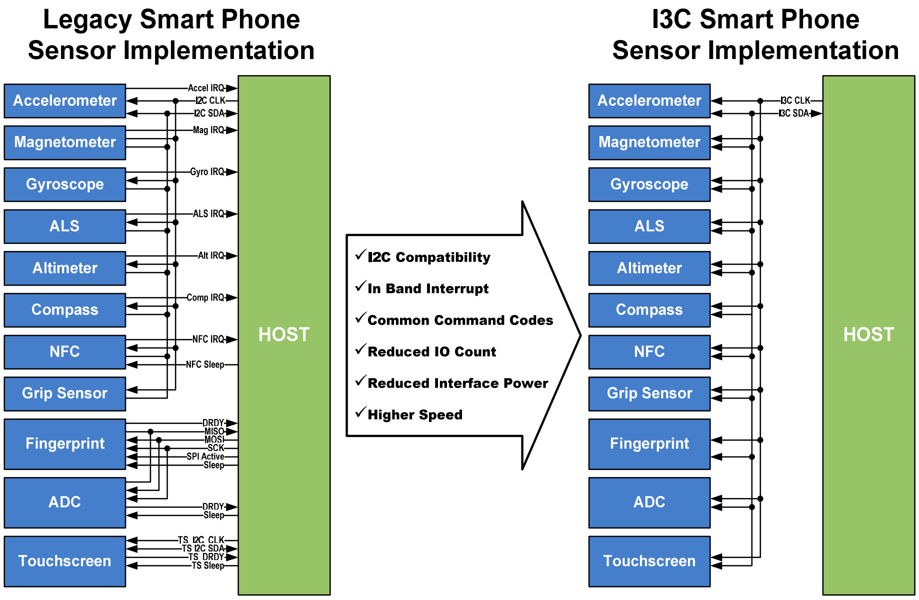

Figure 2. Illustration of typical hardware simplification released with I3C Bus (source: MIPI)

Reduced Power

I2C uses an open drain digital interface with a relatively low-value pull-up resistor. As a result of this topology, every logic “0” transmitted results in a significant amount of current flow through the pull-up resistor. In addition, the low-value pull-up resistance in conjunction with bus capacitance slows digital transitions down significantly, resulting in a low maximum bus speed (the most popular I2C data rates being 400 kHz or 1 MHz). The slow bus speed, in turns, requires that application processors remain active for longer periods of time to empty out slave FIFO buffers that are full of data. Conversely, I3C incorporates a push/pull architecture that results in substantially higher data rates and allows applications processors to communicate with slaves in less time and consume less energy per logic “0.”

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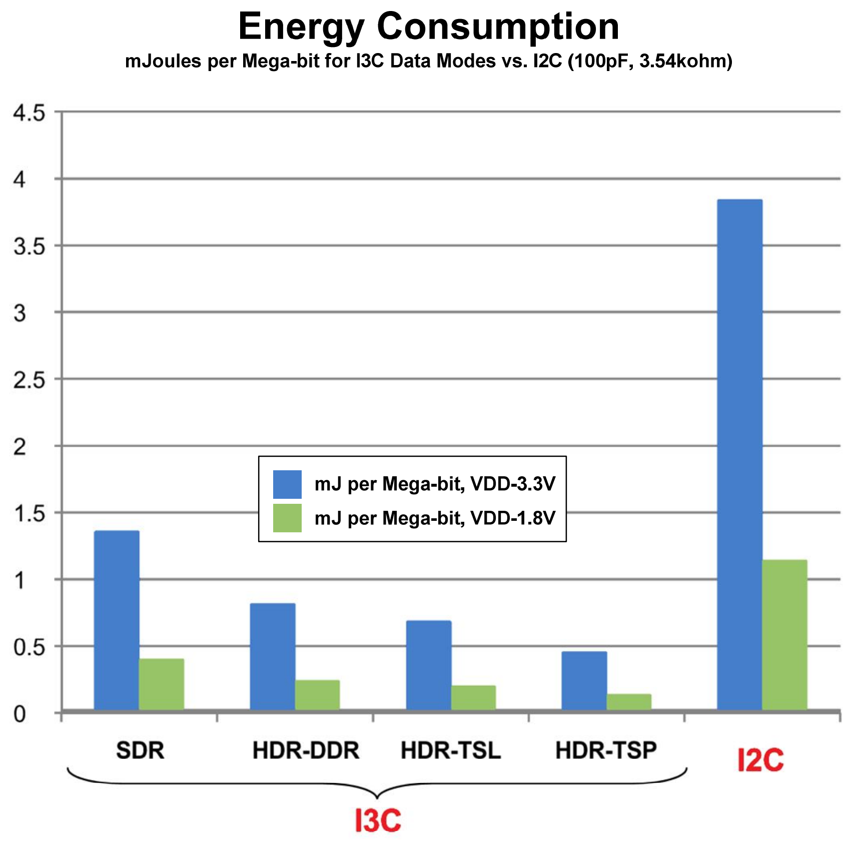

Figure 3. Energy consumption for MIPI I3C modes in comparison to I2C (source: MIPI)

MIPI I3C Key Features

This section presents a high-level overview of the key features of an I3C compatible bus. Details can be obtained in the specification.

Mixed Bus Topologies

As previously mentioned, a key aspect of the I3C specification is its compatibility with legacy I2C devices. This allows new applications to leverage existing I2C devices until a suitable I3C device is available.

Common Command Codes

The I2C bus specification defines the minimum functional requirements, such as how to transmit on the bus and how to address or exchange data, but the specification lacks a protocol definition that supports bus management activities. I3C is a more sophisticated bus that allows masters to maintain control of the bus.

CCCs are the means by which an I3C Master maintains this control. CCCs can be used to communicate with some or all of the Slaves on the I3C bus. The MIPI Alliance defines all CCCs, with few a reserved for future I3C bus

The I3C protocol supports direct “peer-to-peer” communications between slaves, independent of the Master.

enhancements and vendor-specific extensions. Support for a subset of CCCs by Slaves is mandatory, while others are optional, depending upon each device’s capabilities.

CCCs are used by the Master to discover all devices present on the bus, query functional capabilities about those devices, and keep the bus in a consistent operating state.

Dynamic Address Assignment

When an I3C Master discovers a new I3C device on its bus, the device is automatically assigned a dynamic address. This address replaces its default power up static address and becomes its operational address on the bus going forward. The I3C Master can also grant address interrupt priority to slaves with low latency requirements by assigning those devices a low-value dynamic address. In I3C, the lower the dynamic address value, the higher its interrupt priority on the bus.

Broadcast Messages

Every I3C bus supports a standard broadcast address of 0x7E, chosen from the I2C reserve address space to avoid message collisions with legacy I2C Slaves. Broadcast messages allow the Master to issue commands to the entire population of I3C Slaves with a single message.

Peer-to-Peer Messages

The I3C protocol supports direct “peer-to-peer” communications between slaves, independent of the Master. This autonomy allows information to be exchanged between Slaves while the Master is powered down. Not all slaves are required to support peer-to-peer communications.

In-Band Interrupt

In-band Interrupts eliminate the need for a separate pin to signal interrupts. Interrupt arbitration is determined by favoring slave devices with the lowest address, by assigning them a higher bus priority. As discussed previously, In-band Interrupts are a key aspect of the bus to optimize the physical simplicity of the bus.

Hot-Join

The I3C bus protocol supports a Hot-Join mechanism by which Slaves can join the I3C bus, even after it has been fully configured. In order for a Slave to Hot-Join an established network, it must wait for a bus idle condition before introducing itself on the bus.

Power savings can be realized with the Hot-Join feature because it allows certain devices on the bus to be fully powered off during normal bus operation. When these low duty cycle devices powered back on, the I3C Master will readily accept them back onto the network.

Legacy I2C Masters are not capable of supporting the Hot-Join feature, so this functionality would need to be disabled on any I3C Slave before using it on a legacy I2C bus.

In-Band Power Control Messages

The I3C bus defines several activity states as a means for the Master to notify the Slaves about the upcoming levels of activity, or inactivity, on the bus. These activity states help Slaves better manage their individual states in order to save power.

The four activity states (and their expected activity interval) are:

- **Activity State 0**: Normal activity
- **Activity State 1**: Expect no activity for at least 100 µs
- **Activity State 2**: Expect no activity for at least 2 ms
- **Activity State 3**: Expect no activity for at least 50 ms

Error Detection and Recovery

To ensure data integrity, an I3C bus will utilize either simple parity bits or a combination CRC5 encoding along with parity. CRC5 encoding is a cyclic redundancy check with a fifth order polynomial length. CRC5 encoding is only supported by the HDR modes of operation.

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The I3C standard specifies fairly elaborate error detection and recovery methods. When operating in SDR mode, there are seven Slave error types (numbered S0 to S6) and three Master error types (numbered M0 to M2), each with a suggested recovery method. Similarly, a set of errors and recovery methods are defined for each of the HDR operating modes.

Timing Control

Some applications incorporating numerous devices require complex synchronization of activities across the system. I3C buses can achieve accurate system timing by means of synchronous or asynchronous modes operation. It should be noted that the bus is not restricted to just one mode of operation; it is capable of running both modes either independently or concurrently if needed.

- **Synchronous Mode:** The I3C bus achieves timing coordination when the Master issues a period time sync message that Slaves use to align their activities.
- **Asynchronous Modes:** The I3C bus defines four slightly different modes of asynchronous operation. Generally speaking, each asynchronous mode operation allows Slaves to execute their activities autonomously, but asynchronous Slaves will timestamp their data to allow the Master to time-correlate all system data.
    - **Async Mode 0:** Basic mode assumes that a Slave has access to a reasonably accurate and stable clock source for data time stamping – at least accurate for the duration of the time it has to measure. A set of counters, in conjunction with an In-band

    Interrupt, are used to communicate time-stamping information to the Master.
    - **Async Mode 1:** Advanced mode extends the basic mode by using some mutually identifiable bus events like I3C START.
    - **Async Mode 2:** High-precision mode uses SCL falling edges (for SDR and HDR-DDR modes) as a common timing reference for Master and Slave. A burst oscillator is used to interpolate the time between a detected event and next SCL falling edge. For HDR-TSL and HDR-TSP modes, the mode uses both SDA transitions and SCL transitions as a timing reference.
    - **Async Mode 3:** Highest-precision triggerable mode supports precise time triggering and 210 measurements across multiple transducers applications like beamforming.

Multi-Master

The most straightforward I3C bus will incorporate one Primary Master. It is the Primary Master's responsibility to configure the bus. Once bus configuration is established, the Primary Master assumes the role of Current Master.

More sophisticated I3C bus topologies are possible with the addition of Secondary Masters.

More sophisticated I3C bus topologies are possible with the addition of Secondary Masters. As Secondary Masters are introduced to the bus, they will initially present themselves as Slaves and then transition to Masters. Once a Secondary Master is accepted onto the bus, it can request Current Master status. If the Current Master agrees, its Current Master control is handed over to the requesting Secondary Master.

A Secondary Master could prove useful acting as an I3C hub. For example, a Secondary Master may consume much less power than the Primary Master. Thus, the Primary master could be powered down while the Secondary Master collects data from Slaves. Periodically, this data could be relayed onto the Primary Master during its wake-up intervals, leading to significant system power savings.

I2C Features Not Supported in I3C

Although the I3C standard attempts to fully accommodate legacy I2C devices, there are few outlying I2C features that I3C standard does not provide backward compatibility for.

- **Clock Stretching:** All I2C devices are expected to be fast enough to operate at the legacy bus speeds (100 and 400kb/s) supported by I3C.
- **I2C Extended Addresses (10-bits):** All devices on an I3C bus are addressed by a 7-bit address and have a unique 48-bit address which is used only during dynamic address assignments.
- **Pull-Up Resistors:** This component type is no longer used.

Evolution of the I3C Standard

Although the I3C bus standard is new to the electronics industry, it is by no means static. A working group remains active defining new features that future versions of the standard may support. These features will further enhance current functionality and evolve to support future technology and applications.

Possible Future Features

Below is a list of a few of the possible future features have been mentioned on MIPI's website. These features are under consideration by the working group and may not necessarily be approved for future versions of the standard.

- Grouped addressing
- Additional Slave error detection/recovery
- CCC support in HDR-DDR/TSP
- HDR-DDR end write
- HDR-TSP end transfer
- Clock-to-Data refinement
- Timing Control disable
- New minimum t_{IDLE}
- In-Band Hardware Reset (IBHR)
- Multi-Lane, for speed
- HDR-DDR-end CRC

Support for Non-Sensing Applications

In addition to obvious benefits for applications utilizing sensors, there are numerous other mobile applications that the I3C bus could evolve to support. Several MIPI working groups are investigating the possibility of morphing the capabilities I3C standard to suit other application needs. Many of these working groups are listed here along with links to details of their work.

- **Camera Working Group:** Camera Control Interface (CCI) chapter of the MIPI Specification for Camera Serial Interface 2 (CSI-2), v2.1
- **Display Working Group:** Multiple MIPI Specifications for Touch interfaces
- **Debug Working Group:** MIPI Specification for Debug for I3C
- **Reduced I/O (RIO) Working Group:** MIPI Specification for Virtual GPIO Interface

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Figure 4. SignalCraft SCOUT SC4415 Serial Bus Controller

The MIPI-I3C standard offers numerous performance enhancements over I2C and SPI, but these benefits do come at a cost; a substantially more sophisticated electrical interface and protocol. Implementation of this interface could prove daunting; however, these complexities need not deter engineers seeking to leverage the benefits in of incorporating I3C enabled devices in their system. Bring-up of I3C prototype designs or production test systems can easily be streamlined with the SCOUT Serial Bus Controller from SCT. SCOUT is the highest performing, lowest cost I3C capable USB to I3C serial bus adapter on the market.

SCOUT automates the complex and timing critical protocol tasks such as Bus Initialization, Hot Join and Device Priority management. Its physical interfaces have been designed with simplicity and flexibility in mind. Software selectable internal supplies can support logic levels for +1.2V, +1.8V, +2.5V and +3.3V bus operation. Applications requiring custom interface voltages between +0.8V to +3.6V can also be supported with an external voltage source. In addition, SCOUT provides a configurable bus pull-up resistance that automatically connects to the bus when communicating with a legacy I2C devices.

SCOUT was designed with determinism, low latency and fast execution in mind. Timing critical performance obtained using an FPGA architecture and user configurable command cues. Pre-defined command sequences and trigger modes enable multiple executions of each sequences using either software or hardware triggers.

Common applications include 3rd party component evaluation, system integration, troubleshooting and manufacturing test automation.

SCT is working closely with customers and MIPI to provide protocol upgrades and support as the I3C standard evolves and new I3C products emerge on the market.

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